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PERKINS COIE LLP P.O. BOX 1208 SEATTLE, WA 98111-1208			EXAMINER DEWS, BROOKE J	
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**Please find below and/or attached an Office communication concerning this application or proceeding.**

The time period for reply, if any, is set in the attached communication.



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## **DETAILED ACTION**

### ***Response to Amendment***

1. In light of amendment, filed 09/04/2008, the application is still pending. Claims 33-52 and 59 have been cancelled. Applicant's arguments have been fully considered but they are not persuasive, therefore a ***FINAL REJECTION*** is made in view of Frank Barth (US Publication 2003/0191872) and Ichiro Kumata (US Patent 6715010).

### ***Claim Rejections – 35 USC § 102***

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

2. Claims 1-5, 17-21, 53, 55 and 57 are rejected under 35 U.S.C. 102(e) as being anticipated by Frank Barth (US Publication 2003/0191872), hereafter Barth.

**Regarding claims 1-5, 17-21, 53, 55 and 57** Barth discloses disk drive controller for disk drives comprising:

parallel logic (**via port assignment unit 335**) developing parallel control signals (**parallel data signals**); (**Paragraph [0026] and claim 14 of Barth**)

serial logic (**via port assignment unit 335**) developing serial control signals (**serial data signals**);

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and a multiplexer (**via parallel/serial converter 205**) coupling at least one of the parallel control signals (**parallel data signal**) and the serial control signals (**serial data signal**) to at least one of a parallel hard disk drive (**parallel device**) and a first serial hard disk drive (**serial device**) by a common control bus. (**Paragraph [0028-29], Paragraph [0026], and claim 14 of Barth**)

sending data to the first serial hard disk drive and the second serial hard disk drive at effectively double a base data rate (**speed doublings**); (**Paragraph [0005-6]**)

and encoding (**via port map register 340**) additional commands (**port identification data**) onto the common control bus (**same set of host bus addresses**). (**Paragraph [0025 and 0028]**) comprising:

selecting a coding standard; determining an unused coding space of the coding standard;

forcing some of the bits into the unused coding space; and using at least some of the remaining bits of the unused coding space for an additional control communication on the common bus.

### ***Claim Rejections - 35 USC § 103***

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

3. Claims 6-16, 22-31, 54, 56-58, and 60-72 are rejected under 35 U.S.C. 103(a) as being unpatentable over Frank Barth (US Publication 2003/0191872), hereafter Barth in view of Ichiro Kumata (US Patent 6715010), hereafter Kumata.

**Claims 6-8 16, 22, 23, 54, and 56-58** are rejected for the reasons set forth hereinabove for claims 1, 4, 17, 18, 21, 53, and 55, and further Barth discloses wherein:

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the first the parallel hard disk drive (**parallel device**) is an ATA type; (**Claim 1 of Barth**)

the first serial hard disk drive (**serial device**) is an SATA type; (**Claim 1 of Barth**)

the multiplexer (**parallel/serial converter 205**) further coupling at least one of the parallel control signals and the serial control signals to a second serial hard disk drive by the common control bus;

wherein data is sent to the first serial hard disk drive and the second serial hard disk drive at double a base data rate (**speed doublings; Paragraph [0005-6]**), the doubling the base data rate comprising:

Barth does not explicitly disclose developing a sampling data clock; developing a first data stream at the base data rate; developing a second data stream at the base data rate; and multiplexing the first data stream to the common control bus on a rising edge of the base data clock and the second data stream to the common control bus on a falling edge of the base data clock so that the common control bus carries both the first data stream and the second data stream at double the base data rate; and calibrating phases of the first data stream and the second data stream comprising: (a) choosing a phase; (b) testing to see if the phase is accurate; (c) receiving results of the testing; (d) logging the results of the testing; (e) repeating steps (a) through (d) for at least one more phase; (f) finding a threshold rate based on the results of the testing; and (g) dividing the threshold rate by two; and the controller further encoding additional commands onto the common control bus, wherein the encoding comprising: determining at least one invalid command in used coding space of a coding standard; determining unused coding space; and encoding the at least one invalid command in the used coding space and at least one command in the unused coding space; wherein the coding standard is an 8BIOB (8 bit/10 bit) coding standard.

Kumata discloses developing a sampling data clock (**clock signal**); developing a first data stream at the base data rate; developing a second data stream at the base data rate; (**serial transfer paths**) and multiplexing the first data stream to the common control bus on a rising edge of the base data clock and the second data stream to the common control bus on a falling edge of the base data clock so that the common control bus carries both the first data stream and the second data stream at double the base data rate; (**Column 2 lines 50-67**)

and calibrating phases of the first data stream and the second data stream comprising:

(a) choosing a phase; (b) testing to see if the phase is accurate; (c) receiving results of the testing; (d) logging the results of the testing; (e) repeating steps (a) through (d) for at least one more phase; (f) finding a threshold rate based on the results of the testing; and (g) dividing the threshold rate by two; (**Column 18 lines 50-59; Claim 22 of Kumata**)

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and the controller further encoding additional commands onto the common control bus, wherein the encoding comprising:

determining at least one invalid command in used coding space of a coding standard; determining unused coding space; and encoding the at least one invalid command in the used coding space and at least one command in the unused coding space; wherein the coding standard is an 8BIOB (8 bit/10 bit) coding standard. **(Column 21 lines 57-67)**

Kumata and Barth are analogous art because they are from the same field of endeavor involving peripheral configuration.

It would have been obvious to one having ordinary skill in the art to combine the bus emulation methods of Kumata with the system of Barth. The motivation behind such a combination being for a serial transfer path to be optimized for a peripheral circuit requesting a high transfer rate and a peripheral circuit not requesting a high transfer rate. **(Column 22 lines 47-50 of Kumata)**

**Claims 9-15, 24-31, and 60-72** are rejected because the combined limitations have been addressed in the rejected claims above.

### ***Response to Arguments***

4. Applicant's arguments are summarized as the following:

A. Applicant submits that the cited prior art clearly fails to disclose, suggest, or motivate any need for an encoding scheme of the particular type now claimed, and that it would not be obvious to recognize or identify the particular encoding scheme by mere trial because of the vast and potentially unlimited number of encoding schemes available to try.

In response to applicant's argument, **A**, examiner notes that the encoding scheme, mentioned in claim 8, that the applicant refers to is disclosed as a standard coding scheme based from the Serial ATA standard as mentioned not only by the background of the applicant's invention but also Barth discloses the full usefulness of the Serial ATA standard in its background as well **(Paragraph [0006, 0011-0013])**. In Barth the forward and backward compatibility makes its conversion (i.e. coding) obvious.

After further consideration, it appears that the former indication of allowability was prematurely stated.

***Conclusion***

**5. THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Brooke J. Dews whose telephone number is 571-270-1013. The examiner can normally be reached on M-F 6:30-3:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Alford Kindred can be reached on (571) 272-4037. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

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/B. J. D./ 11/18/2008

Examiner, Art Unit 2181

/Alford W. Kindred/

Supervisory Patent Examiner, Art Unit 2181